REMARKS

The Applicants have carefully reviewed and considered the Office Action mailed on April 4, 2006, and the references cited therewith. Claims 1, 9, 15, 22 and 29 have been amended to provide further clarification. No new matter has been entered as a result of the changes made thereto. Reconsideration and allowance of the subject application, as amended, are respectfully requested.

Applicants submitted an Information Disclosure Statement and a 1449 Form on December 26, 2001. Applicants respectfully request that initialed copies of the 1449 Forms be returned to Applicants' Representatives to indicate that the cited references have been considered by the Examiner.

Claims 1-3, 5-6, 9-10, 12, 15-18, 22-23, 25-26 and 29-32 were rejected under 35 USC § 102(b) as being anticipated by Anderson (US 5,898,869). Applicants respectfully traverse this rejection.

In response to arguments made in the Reply filed January 20, 2006, the Office Action has asserted that the "address decode circuitry" disclosed in Anderson meets the limitation "address translation unit" recited in the independent claims 1, 9, 15, 22 and 29. Applicants respectfully disagree and submit that the function of the claimed "address translation unit" is different than the function of the "address decode circuitry" described in Anderson.

Applicants have amended independent claims 1, 9, 15, 22 and 29 to further clarify the function of the "address translation unit." In particular, claims 1, 22 and 29 are amended to recite "setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory ... the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory." Method claims 9 and 15 have similarly been amended to recite "in response to an outbound transaction, converting an internal bus address associated with the outbound transaction to an external data bus address and forwarding the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory."

Support for these amendments may be found in the original specification of the present application, for example, in paragraphs 0028 and 0037.

Applicants respectfully submit that Anderson does not disclose an address translation unit "to enable at least one outbound transaction to address at least one location in the system memory," as recited in the amended claims. The following passage from Anderson describes the function of the address decode circuitry:

> As a further enhancement, the boot logic may be coupled to an address bus received from the host. The boot logic may then include address decode circuitry responsive to a particular address presented by the host for releasing the processor execution and causing the processor to boot. Furthermore, the PCMCIA interface may include a single-chip PCMCIA interface and the address decode circuitry may comprise programmable chip select logic within the single-chip PCMCIA interface. (Anderson, col. 2, lines 46-54) (emphasis added).

Thus, as noted in the Office Action, "the address decode circuitry is set by host so that the processor can be released to begin booting." Address decode circuitry that responds to a particular address presented by the host to release a processor to begin booting is not the same as an address translation unit that is set by a host to enable an outbound transaction to address a location in system memory. Although Anderson discloses that "the boot sequence could include a loader program used to download a program from host 11 to FLASH memory 29," the address decode circuitry merely begins the boot sequence in response to an address presented by a host but does not enable an outbound transaction in the manner recited in the amended claims. The address decode circuitry disclosed by Anderson does not appear to be capable of referencing an outbound transaction to a location on system memory in the host. Moreover, the address decode circuitry disclosed by Anderson does not appear to be capable of converting an internal data bus address to an external data bus address and forwarding an outbound transaction.

Because Anderson fails to disclose each and every element and limitation recited in amended independent claims 1, 9, 15, 22 and 29, applicants submit that these claims, and the claims dependent therefrom, are not anticipated by Anderson. Accordingly, applicants request that the rejection under 35 U.S.C. 102 be withdrawn.

Claims 7, 13, 20, 27 and 34 were rejected under 35 USC § 103(a) as being unpatentable over Anderson (US 5,898,,869) and claims 8, 14, 21, 28 and 35 were rejected under 35 USC §

103(a) as being unpatentable over Anderson (US 5,898,869) in view of Klein (US 6,216,224). Applicants also traverse these rejections.

Dependent claims 2-8, 10-14, 16-21, 23-28 and 30-35 depend, either directly or indirectly, upon amended independent claims 1, 9, 15, 22 and 29. Applicants submit therefore that these dependent claims are patentable by virtue of their dependency, for the reasons stated above, as well as for the additional limitations recited therein.

Accordingly, applicants respectfully submit that all of the claims are in condition for allowance and notification to that effect is earnestly requested.

The Examiner is invited to telephone Applicant's attorney (603-668-6560) to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-2121.

Respectfully submitted,

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By his Representatives,

Customer Number: 45459

603-668-6560

Date 8-4-06

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4 day of AUGUST 2006.

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Name

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Signature